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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,021	11/17/2003	Manoj I. Thadani	884.907US1	5576

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EXAMINER	
PATEL, KAUSHIKKUMAR M	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 08/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/716,021	THADANI, MANOJ I.	
	Examiner	Art Unit	
	Kaushikkumar Patel	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 21* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is in response to applicant's communication filed May 22, 2006 in response to PTO office action mailed March 23, 2006. The applicant's remarks and amendments to the claims were considered with the results that follow.

2. In response to the last office action, claims 1, 5, 8-11, 13-14, 18 and 20-21 have been amended. No claims have been canceled. No new claims have been added. As a result, claims 1-21 remain pending in this application.

Response to Arguments

3. Applicant's arguments with respect to claims 1, 7-8, 13 and 18 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-6, 8-11 13-18 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Murdocca, Miles J. (Principles of Computer Architecture, Prentice Hall, Upper Saddle River, NJ 2000 pg. 270 – 273 and pg. 312) and further in view of Herrell et al. (5,301,287).

1. As per claims 1, 8, and 18, Murdocca teaches:

Mapping, by an operating system (Murdocca pg. 270 7.7.2 lines 1 - 2 "Paging is a form of automatic overlaying that is managed by the operating system"), a range of virtual addresses to a range of physical addresses (Murdocca pg. 270 7.7.2 lines 4 - 5 "...mapping the physical memory address space to some portion of the virtual memory address space..."), wherein a subset of the range of virtual addresses is identity-mapped to a subset of the range of physical addresses (Murdocca pg. 270 Fig. 7-21 clearly shows that virtual addresses 0 – 1023 are identity-mapped to physical memory location 0 – 1023.). Murdocca fails to teach passing a virtual address pointer to DMA module. Herrell teaches passing virtual pointer to DMA device (see abstract, col. 2, line 51 – col. 3, line 39). It would have been obvious to one having ordinary skill in the art at the time of the invention to provide virtual pointer to DMA device as taught by Herrell in the system of Murdocca to provide real time data processing with reduced latency and keeping security of data (see Herrell, col. 2, lines 41-49).

As per claim 2, Murdocca teaches:

The subset of the range of virtual addresses comprises at least a portion of a page table (Murdocca pg. 270 7.7.2 lines 7 – 8 "Eight virtual pages are mapped to four physical page frames." The page 0 subset of the virtual address range is a portion of the page table.)

As per claim 3, Murdocca teaches:

Selecting a start address of the subset of the range of physical addresses; and selecting a size of the subset of the range of physical addresses (An algorithm to reload

data from the physical memory and update the page table are shown in Fig. 7-22 and steps 1 – 4, respectively, on pg. 271. The algorithm allows for any remapping of the page table to occur including mapping any of virtual page addresses 0 – 3 to physical page addresses 0 – 3, respectively, resulting in an identity-mapped memory.)

As per claim 4, Murdocca teaches:

Selecting a number of pages to reserve as the subset of the range of physical addresses (Murdocca pg. 271 gives an algorithm to update the page table and data of each page.)

As per claim 5, Murdocca teaches:

Allocating the subset of the range of physical addresses for use by a direct memory access module (Murdocca pg. 312 8.8.3 lines 15 – 17 "...the CPU programs the DMA device with the starting address in main memory, the starting address in the device and the length of the block to be transferred.")

As per claim 6, Murdocca teaches:

Re-allocating the subset of the range of physical addresses for use by the direct memory access module (Murdocca pg. 270 includes an algorithm for re-allocating virtual-to-physical memory mappings.)

As per claim 9,Murdocca teaches:

Storing application data in the subset of the range of virtual addresses (Murdocca pg. 270 7.7.2 lines 3 – 6 The virtual memory space is used for providing additional data storage.)

As per claim 10, Murdocca teaches:

Determining a need to transfer application data using a direct memory access module (Murdocca pg. 271 Step 1 "A page frame is identified to be overwritten"); and

Storing the application data in the subset of the range of physical addresses by writing the application data to the subset of the range of virtual addresses (Murdocca pg. 271 Step 2 "The virtual page that we want to access is located in secondary memory and is written into physical memory...")

As per claim 11, 14, and 20 - 21, Murdocca teaches:

Transferring application data between the subset of the range of virtual addresses and a peripheral device by passing a virtual pointer associated with the subset of the range of virtual addresses to a direct memory access module (Murdocca pg. 312 8.8.3 lines 15 – 17 "...the CPU programs the DMA device with the starting address in main memory, the starting address in the device and the length of the block to be transferred." Passing the address for transfer requires the use of a pointer to the address as stated in Murdocca pg. 272 lines 2 – 4 of paragraph 1.)

As per claim 13, Murdocca teaches:

A mapped memory having a range of physical addresses (Murdocca pg. 270 7.7.2 lines 4 – 5 "...mapping the physical memory address space..."; and

A register associated with the mapped memory to indicate a subset of a range of virtual addresses that is identity-mapped to a subset of the range of physical addresses (Murdocca pg. 271 includes a programmable page table. Remapping the pages requires registers to hold the translation information.)

As per claim 15, Murdocca teaches:

The peripheral memory comprises a first-in first-out memory (Murdocca pg. 273 lines 6 – 13 of paragraph 2.)

As per claim 16, Murdocca teaches:

A processor associated with a memory map including at least one fixed address included in the range of physical addresses (Murdocca pg. 270 Figs. 7-21 and 7-22 These figures show a mapping scheme with the corresponding page table. The entire range of physical addresses is fixed. The memory disclosed in Murdocca is part of a computer system, which inherently has an associated processor.)

As per claim 17, Murdocca teaches:

A buffer allocated from the subset of the range of physical addresses (Murdocca pg. 131 ¶4 Murdocca discusses a calling scheme which uses a stack. In this calling scheme a portion of the physical memory is used as a buffer.

2. Claim 7 is rejected under **35 U.S.C. 103(a)** as being unpatentable over Murdocca and Herrell as applied to claims 1-6 above, and further in view of U.S. Patent 6,662,272 (Olarig).

3. As per claim 7:

Murdocca does not teach resizing the cache subset of ranges.

Olarig teaches repartitioning the cache partitions into different sizes (Olarig Col. 3 lines 24 – 38 "A partitioned cache can be further optimized by reallocating the sizes of cache partitions...") It would have been obvious to one of ordinary skill in the art at the time of invention to combine this feature of Olarig with Murdocca since the addition of

the feature allows the cache to be optimized according to a set of conditions (Olarig Col. 3 lines 24 – 27.)

4. Claim 12 is rejected under **35 U.S.C. 103(a)** as being unpatentable over Murdocca and Herrell and further in view of U.S. Patent 6,941,390 (Odom).

5. As per claim 12:

Murdocca does not teach transferring application data between a range of virtual addresses and a peripheral device with a FIFO memory.

Odom teaches transferring the data between a data source and a data sink via a buffer (Odom Col. 8 lines 47 – 50.) The buffer is between the data source and the I/O resource (Odom Col. 8 line 64 – Col. 9 line 2.) Odom further teaches that the buffer may be implemented as a FIFO buffer (Odom Col. 9 lines 12 – 19.)

It would have been obvious to one of ordinary skill at the time of the invention to combine this feature of Odom with Murdocca since including the DMA resources allows the DMA controller to configure multiple virtual channels for the I/O devices (Odom Col. 1 lines 51 – 55.) Included among the DMA resources is the buffer that may be configured as a FIFO buffer coupled to the data source (Odom Col. 7 lines 4 – 16.)

6. Claim 19 is rejected under **35 U.S.C. 103(a)** as being unpatentable over Murdocca and Herrell and further in view of U.S. Patent 5,659,798 (Blumrich et al.)

7. As per claim 19:

Murdocca does not teach using a graphics frame buffer.

The use of graphics frame buffers is common in the art. It would have been obvious to one of ordinary skill in the art at the time of invention to include a graphics frame buffer to provide graphics capabilities as evidenced by the use of a graphics frame buffer in a virtual addressing environment in Blumrich (Blumrich Col. 18 lines 22 – 26.)

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaushikkumar Patel whose telephone number is 571-272-5536. The examiner can normally be reached on 8.00 am - 4.30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kaushikkumar Patel
Examiner
Art Unit 2188

kmp

8/6/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER